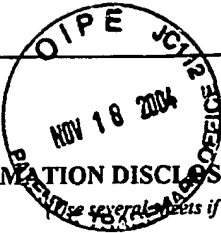| FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500395.02	APPLICATION NO. 09/758,970

INFORMATION DISCLOSURE STATEMENT
(Use several sheets if necessary)

APPLICANT(S) Ronnie M. Harrison	
FILING DATE January 9, 2001	GROUP ART UNIT ~~2819~~ 2816

(OIPE JC1/2 stamp: NOV 18 2004)

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
HLN	AA	5,666,313	09/09/97	Ichiguchi	365	195	
HLN	AB	6,484,244 B1	11/19/02	Manning	711	154	
	AC						
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	NO
	AK							
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	AN							
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OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

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INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Ronnie M. Harrison	
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U.S. PATENT DOCUMENTS

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	AA						
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
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	AP	Park, D. et al., "Fast Acquisition Frequency Synthesizer with the Multiple Phase Detectors", IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Vol. 2, May 1991. pp. 665-668.
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INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANTS Ronnie M. Harrison	
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
HLN	HA	6,005,823	12/21/99	Martin et al.	365	230.08	
	HB	6,011,732	01/04/00	Harrison et al.	365	194	
	HC	6,016,282	01/18/00	Keeth	365	233	
	HD	6,026,050	02/15/00	Baker et al.	635	233	
	HE	6,029,250	02/22/00	Keeth	713	400	
	HF	6,038,219	03/14/00	Mawhinney et al.	370	242	
	HG	6,067,592	05/23/00	Farmwald et al.	710	104	
	HH	6,101,152	08/08/00	Farmwald et al.	365		
	HI	6,101,197	08/08/00	Keeth et al.	370	517	
	HJ	6,105,157	08/15/00	Miller	714	744	
	HK	6,160,423	12/12/00	Haq	327	41	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	NO
HLN	HL	0 171 720 A2	02/19/86	EP			X	
	HM	6-1237512	10/22/86	JP (Abstract Only)			X	
	HN	0 295 515 A1	12/21/88	EP			X	
	HO	2-112317	4/25/90	JP (+ Abstract)				X
	HP	0 406 786 A1	1/9/91	EP			X	
	HQ	0 450 871 A2	10/9/91	EP			X	
	HR	0 476 585 A3	3/25/92	EP			X	
	HS	4-135311	5/8/92	JP (+ Abstract)				X
	HT	5-136664	6/1/93	JP (+ Abstract)				X
	HU	5-282868	10/29/93	JP (Abstract Only)			X	
	HV	WO 94/29871	12/22/94	PCT			X	

EXAMINER *Hailong Nguyen*	DATE CONSIDERED 04/28/2005

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APPLICANTS
Ronnie M. Harrison

FILING DATE
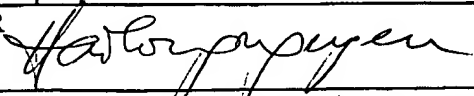January 9, 2001

GROUP ART UNIT 2816
~~Not Yet Assigned~~

HZN	HW	0 655 741 A2	5/31/95	EP		—	—	X	
HZN	HX	0 655 834 A1	5/31/95	EP		—	—	X	
	HY	WO 95/22200	8/17/95	PCT		—	—	X	
	HZ	WO 95/22206	8/17/95	PCT		—	—	X	
	IA	0 680 049 A2	11/2/95	EP		—	—	X	
	IB	0-7319577	12/8/95	JP (Abstract Only)		—	—	X	
	IC	0 703 663 A1	3/27/96	EP		—	—	X	
	ID	0 704 848 A3	4/3/96	EP		—	—	X	
	IE	0 704 975 A1	4/3/96	EP		—	—	X	
	IF	WO 96/10866	4/11/96	PCT		—	—	X	
	IG	0 767 538 A1	4/9/97	EP		—	—	X	
	IH	WO 97/14289	4/24/97	PCT		—	—	X	
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HZN	IJ		Alvarez, J. et al. "A Wide-Bandwidth Low Voltage PLL for PowerPC [TM] Microprocessors" IEEE IEICE Trans. Electron., Vol. E-78. No. 6, June 1995, pp. 631-639
	IK		Anonymous, "400MHz SLDRAM, 4M X 16 SLDRAM Pipelined, Eight Bank, 2.5 V Operation," SLDRAM Consortium Advance Sheet, published throughout the United States, pp.1-22
	IL		Anonymous, "Draft Standard for a High-Speed Memory Interface (SyncLink)", Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-56
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	IO		Anonymous, "Variable Delay Digital Circuit", IBM Technical Disclosure Bulletin, Vol. 35, No. 4A, September 1992, pp. 365-366

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	04/28/05

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APR 3 0 2001

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	IP	Arai, Y. et al., "A CMOS Four Channel x 1K Time Memory LSI with 1-ns/b Resolution", IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, M, 8107 March, 1992, No. 3, New York, US, pp. 359-364 and pp. 528-531	
	IQ	Arai, Y. et al., "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", XP 000597207, IEEE Journal of Solid-State Circuits, Vol. 31, No.2, February 1996, pp. 212-220	
	IR	Aviram, A. et al., "OBTAINING HIGH SPEED PRINTING ON THERMAL SENSITIVE SPECIAL PAPER WITH A RESISTIVE RIBBON PRINT HEAD", IBM Technical Disclosure Bulletin, Vol. 27, No. 5, October 1984, pp. 3059-3060	
	IS	Bazes, M., "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, February 1991, pp. 165-168	
	IT	Chapman, J. et al., "A Low-Cost High-Performance CMOS Timing Vernier for ATE", IEEE International Test Conference, Paper 21.2, 1995, pp. 459-468	
	IU	Cho, J. "Digitally-Controlled PLL with Pulse Width Detection Mechanism for Error Correction", ISSCC 1997, Paper No. SA 20.3, pp. 334-335	
	IV	Christiansen, J., "An Integrated High Resolution CMOS Timing Generator Based on an Array of Delay Locked Loops", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 952-957	
	IW	Combes, M. et al., "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 958-965	
	IX	Donnelly, K. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, December 1996, pp. 1995-2001	
	IY	Goto, J. et al., "A PLL-Based Programmable Clock Generator with 50- to 350-MHz Oscillating Range for Video Signal Processors", IEICE Trans. Electron., Vol. E77-C, No. 12, December 1994, pp. 1951-1956	
	IZ	Gustavsion, David B., et al., "IEEE Standard for Scalable Coherent Interface (SCI)," IEEE Computer Society, IEEE Std. 1596-1992, August 2, 1993.	
	JA	Hamamoto, T., "400-MHz Random Column Operating SDRAM Techniques with Self-Skew Compensation", IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 770-778	
	JB	Ishibashi, A. et al., "High-Speed Clock Distribution Architecture Employing PLL for 0.6μm CMOS SOG", IEEE Custom Integrated Circuits Conference, 1992, pp. 27.6.1-27.6.4	
	JC	Kim, B. et al., "A 30MHz High-Speed Analog/Digital PLL in 2μm CMOS", ISSCC, February 1990	

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APR 3.9 2001

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JD	Kikuchi, S. et al., "A GATE-ARRAY-BASED 666MHz VLSI TEST SYSTEM", IEEE International Test Conference, Paper 21.1, 1995, pp. 451-458	
JE	Ko, U. et al., "A 30-ps JITTER, 3.6-µs LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4	
JF	Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No. FA 18.6, 1994, pp. 300-301	
JG	Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429	
JH	Ljuslin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629	
JI	Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732	
JJ	Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123	
JK	Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997	
JL	Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266	
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JN	Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291	
JO	Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50.	
JP	Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690.	
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JR	Sidiropoulos, S. et al., "A Semi-Digital DLL with Unlimited Phase Shift Capability and 0.08-400MHz Operating Range," IEEE International Solid State Circuits Conference, February 8, 1997, pp.332-333	
JS	Soyuer, M. et al., " A Fully Monolithic 1.25GHz CMOS Frequency Synthesizer", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 127-128	
JT	Taguchi, M. et al., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 1991, pp. 1493-1497	
JU	Tanoi, S. et al., "A 250-622 MHz Deskew and Jitter-Suppressed Clock Buffer Using a Frequency- and Delay-Locked Two-Loop Architecture", 1995 Symposium on VLSI Circuits Digest of Technical Papers, Vol. 11, No. 2, pp. 85-86	
JV	Tanoi, S. et. al., "A 250-622 MHz Deskew and Jitter-Suppressed Clock Buffer Using Two-Loop Architecture", IEEE IEICE Trans. Electron., Vol.E-79-C. No. 7, July 1996, pp.898-904	
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